Repeated epitaxial growth and transfer of arrays of patterned, vertically aligned, crystalline Si wires from a single Si(111) substrate

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Multiple arrays of Si wires were sequentially grown and transferred into a flexible polymer film from a single Si(111) wafer. After growth from a patterned, oxide-coated substrate, the wires were embedded in a polymer and then mechanically separated from the substrate, preserving the array structure in the film. The wire stubs that remained were selectively etched from the Si(111) surface to regenerate the patterned substrate. Then the growth catalyst was electrodeposited into the holes in the patterned oxide. Cycling through this set of steps allowed regrowth and polymer film transfer of several wire arrays from a single Si wafer. © *2008 American Institute of Physics*.
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Silicon nanowires and microwires have been fabricated by the selective wet etching[1] and reactive ion etching[2] of planar Si wafers, or by chemical vapor deposition (CVD) without patterning the substrate,[3] with lithographic patterning of the substrate,[4] with patterning by alumina masking,[5] and with confinement of the wire growth within alumina templates.[6,7] The CVD methods generally involve wire growth by a vapor-liquid-solid (VLS) mechanism, in which a catalyst metal forms a eutectic mixture with Si to induce heterogeneous decomposition of gas precursors to promote one-dimensional growth, usually in the ⟨111⟩ direction.[8,9] Transmission electron microscope (TEM) studies have shown that epitaxial VLS growth from a crystalline Si(111) substrate yields Si wires that are highly crystalline.[10,11] Although the use of templates[6,12] or nonepitaxial growth methods[13] obviate the use of single crystal substrates, the resulting Si wires are either very small and/or poorly aligned. We report herein the repeated VLS-catalyzed growth of large-area arrays of single crystalline, vertically oriented, Si wires from a single patterned Si(111) wafer.

The first-generation Si wire arrays were fabricated by epitaxial VLS growth on a Si wafer.[4] A Si(111) wafer (330–430 μm thick *n*-type Si, doped with Sb to a resistivity of 0.005–0.02 Ω cm, International Wafer Service, Inc.) with 300 nm of a thermally grown silicon oxide was photolithographically patterned with S1813 photoresist (Microchem), followed by immersion for 4 min in buffered HF(aq) (Transene, Inc., 9% HF, 32% NH_4F) to remove the oxide in the holes formed by exposure of the photoresist. Au (300 nm) was then thermally evaporated onto the wafer, followed by lift-off of the remaining resist. Lithographic patterning resulted in a square array of 3 μm diameter Au islands, having a center-to-center pitch of 7 μm, separated by the SiO_2 layer. The wafers were then annealed in a tube furnace at 1000 °C for 20 min under 1 atm of H_2 at a flow rate of 1000 standard $cm^3\ min^{-1}$ (SCCM), and then wire growth proceeded during a subsequent 30 min step by addition of a flow of 20 SCCM of $SiCl_4$ while maintaining the same pressure, temperature, and H_2 flow rate. This process produced highly uniform, vertically aligned, crystalline Si wires over large areas (>1 cm^2) [Fig. 1(a)]. The wire array dimensions and pore spacing used in this work were chosen based on an available lithography mask, to facilitate comparison to previous results.[4] Other wire diameters and center-to-center pitches could be produced by the use of other masks, to the limit of the resolution and pore-size fidelity that can be accommodated by the development and etching steps. The optimal catalyst volume is readily calculated for a given wire radius from the surface tension of the Au meniscus on the growing Si wire.[8,9] The SiO_2 buffer layer had a thickness approximately equal to that of the deposited metal.

A 10:1 (by weight) ratio of polydimethylsiloxane (PDMS) and a curing agent (Sylgard® 184 from Dow Corning) was applied to the top of the wire array either by drop casting or by spin coating at low rpm. The sample was then heated for 2 h at 120 °C to cure and solidify the polymer. Scanning electron microscopy (SEM) images confirmed that the PDMS fully infiltrated the Si wire array. The polymer film and the embedded Si wires were then removed by scraping the wafer surface with a razor blade [Fig. 1(b)]. This transfer approach preserved the pattern fidelity and vertical alignment of the wires within the polymer matrix.[14]

After the removal of the PDMS layer, residual stubs of broken Si wires, 2 μm long or less, along with some polymer residue, were observable at the wafer surface [Fig. 1(c)]. To enable wire regrowth, the wafers were immersed for 90 s in stirred 4.5*M* KOH(aq) at 80 °C.[15] At elevated temperatures, KOH(aq) etches the Si(100) and (110) planes approximately two orders of magnitude faster than it etches the Si(111) plane. Furthermore, the etch rate for Si is significantly faster than that for SiO_2.[15] The KOH(aq) thus selectively etched the Si stubs as well as the polymer residue. After etching, the original oxide hole pattern remained, with the Si(111) substrate exposed at the bottom of each hole [Fig. 1(d)].

Electrodeposition was then used to redeposit the VLS catalyst into the holes in the oxide. The oxide was removed from the back surface of the Si by etching the back for 5 min with buffered HF(aq). Care was taken during this step to

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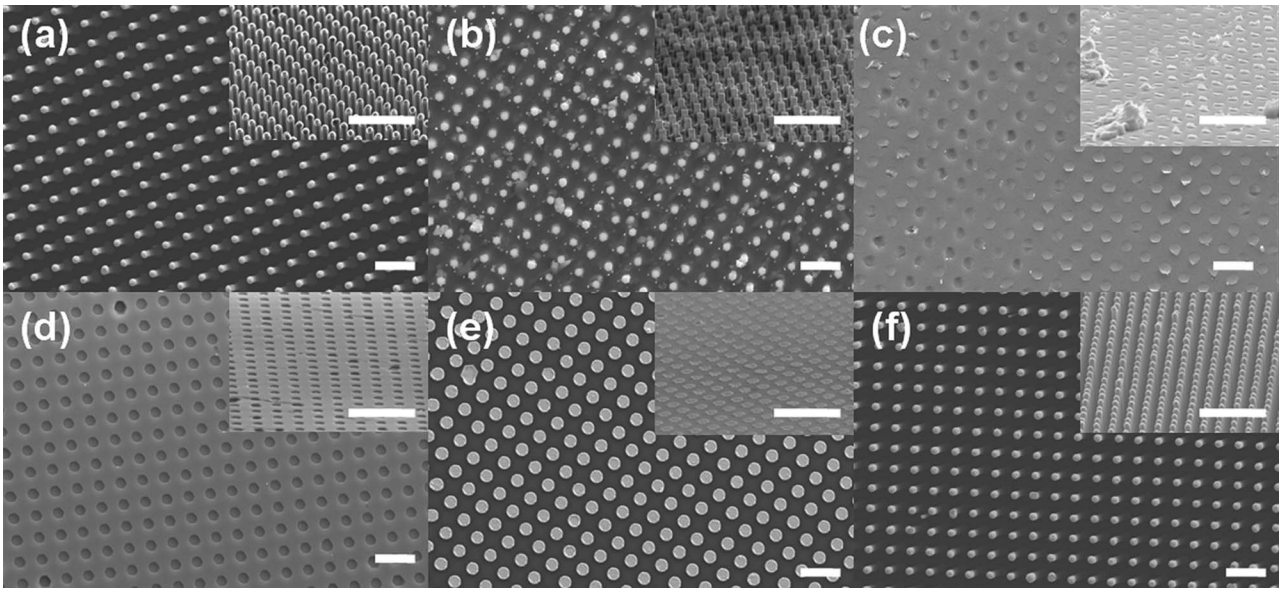

FIG. 1. Top-down and 70° tilted view (insets) SEM images of the wire array regrowth process. The first-generation wire array (a) was peeled in PDMS (b), leaving behind a wafer surface with wire stubs and polymer residue (c). The oxide pattern was recovered with a KOH(aq) etch (d). Au catalyst was electrodeposited into the holes (e). A wire array was regrown from the wafer (f). The scale bar is 10 μm for the top-down images and 20 μm for the inset images.

avoid any contact between the HF(aq) and the front surface of the wafer. A piece of two-sided, conductive Cu tape was then attached to the back of the wafer. The assembly was made into an electrode by connecting the other side of the Cu tape to a Cu wire that was sealed in a glass tube. Mounting wax was used to seal the tube and cover the wafer, so that only the patterned oxide on the front of the wafer was exposed. This electrode was then dipped in 10% (by volume) HF(aq) for 10 s to remove the native oxide at the bottom of the patterned holes. The electrode was thoroughly rinsed in H_2O and then immediately transferred to a Au electrodeposition bath (Orotemp 24 from Technic, Inc.). Relatively low current densities (0.4–0.8 mA cm^{-2} of exposed wafer area between the Si working electrode and the Pt gauze counterelectrode) and Si wafers of high conductivity were required to electrodeposit uniform layers of Au selectively inside the oxide pattern [Fig. 1(e)]. The deposition was allowed to proceed galvanostatically until 0.12 C cm^{-2} of charge had been passed, yielding Au catalyst arrays of 3 μm diameter and approximately 300 nm thickness over areas >1 cm^2. With sufficiently deep pores, no limit has yet been observed for the thickness of Au that can be homogeneously deposited by the electroplating method. The wafer, with metal catalyst deposits in the patterned holes in the oxide layer, was then recovered from the electrode by thoroughly dissolving the mounting wax in acetone.

This substrate was then placed back into the reactor for VLS-catalyzed wire growth, under the same conditions used to grow the first-generation Si wire arrays on the Si(111) substrate, including the 20 min annealing step. The regrown Si wires were between 70 and 100 μm long, with the wires in any single growth run of a uniform height distribution. The entire process was repeated to fabricate a third and fourth generation of wires. No appreciable differences in wire length, diameter, vertical orientation, or morphology were detected between growth generations.

Defects, defined as a Si wire missing from the pattern, were evaluated using imaging software surveys of top-down SEM views of the wire arrays. Because every defect in the surface pattern was transferred to succeeding generations, the success of subsequent growths depended directly on the quality of the initial array. The oxide template served the crucial role of preserving the pattern fidelity by preventing the catalyst metal from migrating across the wafer surface during the growth reaction.[4] Second-generation wire arrays were nearly defect free [Fig. 1(f)]. However, damage to the oxide pattern, caused by the formation of HCl in the reactor,[11] and undercutting during the KOH etch, was observed to introduce defects in the wire array. The accumulation of defects became more prominent, although still fairly modest, in third-generation and fourth-generation arrays (Fig. 2 and Table I). In the fourth-generation arrays, the number of defects approached 10% of the initial wire density. With the optimization of the reaction process, it is likely that the density of defects could be reduced, so that several more generations of useful wire arrays could be produced with the

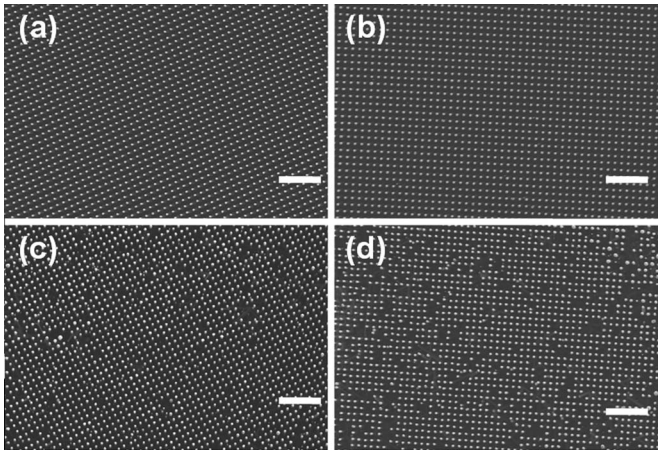

FIG. 2. Top-down SEM images for first-generation (a), second-generation (b), third-generation (c), and fourth-generation (d) Si wire arrays, showing increasing defect density with successive generations of wire growth using a single oxide pattern on the substrate. The scale bar in each image is 40 μm.

TABLE I. Average defect density within each generation of arrays.[a]

Wire array generation	Defect density (cm^{-2})	Defect percentage (%)
First	$(7.5 \pm 5.0) \times 10^2$	0.04 ± 0.02
Second	$(2.5 \pm 1.1) \times 10^4$	1.2 ± 0.5
Third	$(1.4 \pm 0.7) \times 10^5$	6.6 ± 3.4
Fourth	$(2.2 \pm 0.8) \times 10^5$	10.0 ± 3.4

[a]The data were collected using five top-down view SEM images of each generation. The averages were weighted by the area surveyed within each image.

same oxide pattern. The use of ethylenediamine pyrocatechol instead of KOH ought to further improve the selectivity of etching Si relative to SiO_2.[16]

Wire regrowth on a single Si(111) substrate was further extended by subjecting cycled wafers to mechanical polishing, which reduced their thickness by 10–20 μm, followed by thermal oxidation. To simulate rapid and inexpensive processing, the wafers were intentionally polished in a cursory manner. Because restoration of the patterned oxide overlayer required oxidation and then etching of the Si wafer, some degree of surface roughness should be tolerable. The polished Si wafers were thermally oxidized in a tube furnace under a fully hydrated atmosphere of industrial grade air at 900 °C for 8 h, resulting in a 300–400 nm thick surface oxide. Even with an imperfect starting surface, VLS-catalyzed wire growth yielded a vertically aligned Si wire array of comparable quality to that of the first-generation Si wire array (Fig. 3).

Even without further improvements, if four generations of arrays can be grown from each oxide template and only 10 μm of wafer thickness is lost in each polishing step, a single 400 μm thick wafer would be capable of producing 160 Si wire arrays (fewer, if the wafer thinness limits its manipulation). Reasonable expectations for optimization (i.e., five generations per oxide layer, and 2 μm of Si removed per polishing step) imply that the same thickness of Si substrate should be capable of producing 1000 or more Si wire arrays. Furthermore, the VLS growth catalyst can be replaced by Ni or Cu to produce Si wire arrays of nominally equivalent structure[4,14] that ought to have superior electronic properties relative to those produced from the deep-trap Au VLS catalyst. Given the proven low cost of chlorosilane-based CVD processes,[17,18] the approach described herein has the potential to afford a scalably manufacturable method for the production of large areas of oriented, patterned Si wire arrays for use in solar cells, batteries, photonics, and a variety of other applications.

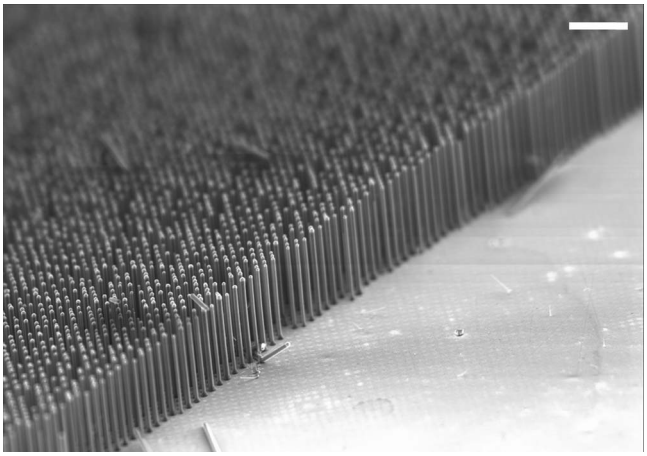

FIG. 3. Tilted view SEM image of a Si wire array grown from a Si(111) wafer that had been mechanically polished and then thermally oxidized. The scale bar is 40 μm.

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